We claim:

1) A combiner processor comprising:

a sliding correlator for correlating a serial stream of baseband symbols against a first codeword and forming a correlation peak output;

a training decision function coupled to said correlation peak output and generating a window output and a training decision output;

a demultiplexer coupled to said correlation peak output and having a learn control input whereby when said demultiplexer learn control input is asserted:

said correlation peak output is coupled to a channel profile memory such that said correlation peak output is added to said channel profile memory when said training decision output is true and said correlation peak output is inverted and added to said channel profile memory when said training decision is false;

and when said demultiplexer learn control input is not asserted:

said correlation peak output is multiplied with the complex conjugate of said channel profile memory and coupled to an accumulator which adds said multiplier result during each said window and generates a decision output at the end of each said window.

2) The combiner processor of claim 1 where said first codeword is 11 bits.

3) The combiner processor of claim 1 where said first codeword is a Barker codeword.

4) The combiner processor of claim 1 where said first codeword is {+1,-1,+1,+1,-1,+1,+1,+1,-1,-1,-1}.

5) The combiner processor of claim 1 where said first codeword is {-1,+1,-1,-1,+1,-1,-1,-1,+1,+1,+1}.

6) The combiner processor of claim 1 where said serial stream of baseband symbols includes Barker codewords.

7) The combiner processor of claim 1 where said serial stream of baseband symbols is quadrature.

8) The combiner processor of claim 7 where said serial stream of quadrature symbols includes an I channel and a Q channel.

9) The combiner processor of claim 1 where said training decision function window output has duration equal to the duration of said codeword.

10) The combiner processor of claim 1 where said training decision function window output includes pre-cursor symbols arriving prior to the largest said correlation peak in said window.

11) The combiner processor of claim 1 where said training decision function window includes post-cursor symbols arriving after the largest said correlation peak in said window.

12) The combiner processor of claim 1 where said training decision output indicates which said codeword was received during said window.

13) The combiner processor of claim 1 where said demultiplexer learn input is asserted during a first interval.

14) The combiner processor of claim 13 where said first interval occurs during the preamble of a received packet.

15) The combiner processor of claim 13 where said first interval is greater than 10 said codeword symbols.

16) The combiner processor of claim 1 where said complex conjugate comprises negating the value of the Q channel.

17) The combiner processor of claim 1 where said channel profile memory is synchronized to said training decision function window output.

18) The combiner processor of claim 1 where said channel profile memory comprises a random access memory and a memory controller coupled to said random access memory.

19) The combiner processor of claim 1 where said channel profile memory adds quadrature said correlation peak output when said demultiplexer learn input is asserted.

20) The combiner processor of claim 1 where said channel profile memory is initialized when said demultiplexer learn control input is first asserted.

21) The combiner processor of claim 1 where said channel profile memory has a number of locations equal to the number of samples in said codeword.

22) The combiner processor of claim 1 where said accumulator includes a memory which is initialized at the start of each said window.

23) The combiner processor of claim 1 where said accumulator includes a memory and an adder which adds the current said multiplier output to said memory contents.

24) The combiner processor of claim 1 where said decision output compares said accumulated value against a threshold at the end of said window.

25) The combiner processor of claim 24 where said threshold is 0.

26) A combiner processor having two states:

a training state whereby a serial stream of baseband symbols is correlated against a first codeword, thereby producing a correlation peak output, said correlation peaks examined by a training decision function to generate a window output indicating the extent of said symbol and a

decision output which is either true or false, said correlation peaks added to a channel profile memory when said decision output is true and inverted and added to said channel profile memory when said decision output is false;

a decision state whereby said serial stream of baseband symbols is multiplied by the complex conjugate of the contents of said channel profile memory to produce a multiplier output;

an accumulator coupled to said multiplier output whereby said adder is reset at the start of said window, accumulates the output of said multiplier during said window, and generates a binary output value at the end of said window.

27) The combiner processor of claim 26 where said first codeword is 11 bits.

28) The combiner processor of claim 26 where said first codeword is a Barker codeword.

29) The combiner processor of claim 26 where said first codeword is {+1,-1,+1,+1,-1,+1,+1,+1,-1,-1,-1}.

30) The combiner processor of claim 26 where said first codeword is {-1,+1,-1,-1,+1,-1,-1,-1,+1,+1,+1}.

31) The combiner processor of claim 26 where said serial stream of baseband symbols includes Barker codewords.

32) The combiner processor of claim 26 where said serial stream of baseband symbols is quadrature.

33) The combiner processor of claim 32 where said serial stream of quadrature symbols includes an I channel and a Q channel.

34) The combiner processor of claim 26 where said training decision function window output has duration equal to the duration of said codeword.

35) The combiner processor of claim 26 where said training decision function window output includes pre-cursor symbols arriving prior to the largest said correlation peak in said window.

36) The combiner processor of claim 26 where said training window includes post-cursor symbols arriving after the largest said correlation peak in said window.

37) The combiner processor of claim 26 where said training decision output indicates which said codeword was received during said window.

38) The combiner processor of claim 26 where said training state occurs during a first interval.

39) The combiner processor of claim 38 where said first interval occurs during the preamble of a received packet.

40) The combiner processor of claim 38 where said first interval is greater than 10 said codeword symbols.

41) The combiner processor of claim 26 where said complex conjugate comprises negating the value of the Q channel.

42) The combiner processor of claim 26 where said channel profile memory is synchronized to said training decision function window output.

43) The combiner processor of claim 26 where said channel profile memory comprises a random access memory and a memory controller coupled to said random access memory.

44) The combiner processor of claim 26 where said channel profile memory adds quadrature said correlation peak output when said demultiplexer learn input is asserted.

45) The combiner processor of claim 26 where said channel profile memory is initialized at the beginning of said training state.

46) The combiner processor of claim 26 where said channel profile memory has a number of locations equal to the number of samples in said codeword.

47) The combiner processor of claim 26 where said accumulator includes a memory which is initialized at the start of each said window.

48) The combiner processor of claim 26 where said accumulator includes a memory and an adder which adds the current said multiplier output to said memory contents.

49) The combiner processor of claim 26 where said binary output compares said accumulated value against a threshold at the end of said window.

50) The combiner processor of claim 49 where said threshold is 0.

51) The combiner processor of claim 26 where said decision state occurs during a second interval.

52) A process for generating a decision output from a serial stream of baseband symbols, said process comprising:

a first learning step comprising:

correlating said incoming serial stream with one or more codewords to generate a correlation output, examining the said correlation output to generate a training decision which is positive or negative, and also generating a window signal indicating the start and end of said incoming symbols, said incoming symbols added to a channel profile memory when said training decision is positive, and inverting said incoming symbols and adding to said channel profile memory when said training decision is negative;

a second decision step comprising:

multiplying said correlation peaks with the complex conjugate of said channel profile memory contents, thereby forming a multiplier output and accumulating said multiplier output during said window start time to said window end time to form a decision value, and comparing said decision value at the said window end time to form said decision output.

53) The process of claim 52 where said first codeword is 11 bits.

54) The process of claim 52 where said first codeword is a Barker codeword.

55) The process of claim 52 where said first codeword is {+1,-1,+1,+1,-1,+1,+1,+1,-1,-1,-1}.

56) The process of claim 52 where said first codeword is {-1,+1,-1,-1,+1,-1,-1,-1,+1,+1,+1}.

57) The process of claim 52 where said serial stream of baseband symbols includes Barker codewords.

58) The process of claim 52 where said serial stream of baseband symbols is quadrature.

59) The combiner processor of claim 7 where said serial stream of quadrature symbols includes an I channel and a Q channel.

60) The process of claim 52 where said window output has duration equal to the duration of said codeword.

61) The process of claim 52 where said window output includes pre-cursor symbols arriving prior to the largest said correlation peak in said window.

62) The process of claim 52 where said window includes post-cursor symbols arriving after the largest said correlation peak in said window.

63) The process of claim 52 where said training decision output indicates which said codeword was received during said window.

64) The process of claim 52 where said learning step precedes said decision step.

65) The process of claim 52 where said learning step occurs during the preamble of a received packet.

66) The process of claim 52 where said learning step uses more than 10 said codeword symbols.

67) The process of claim 52 where said complex conjugate comprises negating the value of the Q channel.

68) The process of claim 52 where said channel profile memory is synchronized to said window.

69) The process of claim 52 where said channel profile memory comprises a random access memory and a memory controller coupled to said random access memory.

70) The process of claim 52 where said channel profile memory adds quadrature said correlation peak output during said learning step.

71) The process of claim 52 where said channel profile memory is initialized at the beginning of said learning step.

72) The process of claim 52 where said channel profile memory has a number of locations equal to the number of samples in said codeword.

73) The process of claim 52 where said accumulation includes a memory which is initialized at the start of each said window.

74) The process of claim 52 where said accumulation includes a memory and an adder which adds the current said multiplier output to said memory contents.

75) The process of claim 52 where said decision value compares said accumulated value against a threshold at the end of said window.

76) The combiner processor of claim 24 where said threshold is 0.

77) A combiner processor comprising:

a sliding correlator for correlating a serial stream of baseband symbols against a first codeword and forming a correlation peak output;

a training decision function coupled to said correlation peak output and generating a window output and a training decision output;

said correlation peak output is coupled to a channel profile memory such that said correlation peak output is added to said channel profile memory when said training decision output is true and said correlation peak output is inverted and added to said channel profile memory;

a decision control input whereby when said decision control input is asserted, said correlation peak output is multiplied with the complex conjugate of said channel profile memory and coupled to an accumulator which adds said multiplier result during each said window and generates a decision output at the end of each said window.

78) The combiner processor of claim 77 where said first codeword is 11 bits.

79) The combiner processor of claim 77 where said first codeword is a Barker codeword.

80) The combiner processor of claim 77 where said first codeword is {+1,-1,+1,+1,-1,+1,+1,+1,-1,-1,-1}.

81) The combiner processor of claim 77 where said first codeword is {-1,+1,-1,-1,+1,-1,-1,-1,+1,+1,+1}.

82) The combiner processor of claim 77 where said serial stream of baseband symbols includes Barker codewords.

83) The combiner processor of claim 77 where said serial stream of baseband symbols is quadrature.

84) The combiner processor of claim 7 where said serial stream of quadrature symbols includes an I channel and a Q channel.

85) The combiner processor of claim 77 where said training decision function window output has duration equal to the duration of said codeword.

86) The combiner processor of claim 77 where said training decision function window output includes pre-cursor symbols arriving prior to the largest said correlation peak in said window.

87) The combiner processor of claim 77 where said training decision function window includes post-cursor symbols arriving after the largest said correlation peak in said window.

88) The combiner processor of claim 77 where said training decision output indicates which said codeword was received during said window.

89) The combiner processor of claim 77 where said decision input is not asserted during a first interval.

90) The combiner processor of claim 89 where said first interval occurs during the preamble of a received packet.

91) The combiner processor of claim 89 where said first interval is greater than 10 said codeword symbols.

92) The combiner processor of claim 77 where said complex conjugate comprises negating the value of the Q channel.

93) The combiner processor of claim 77 where said channel profile memory is synchronized to said training decision function window output.

94) The combiner processor of claim 77 where said channel profile memory comprises a random access memory and a memory controller coupled to said random access memory.

95) The combiner processor of claim 77 where said channel profile memory adds quadrature said correlation peak output at all times.

96) The combiner processor of claim 77 where said channel profile memory is initialized.

97) The combiner processor of claim 77 where said channel profile memory has a number of locations equal to the number of samples in said codeword.

98) The combiner processor of claim 77 where said accumulator includes a memory which is initialized at the start of each said window.

99) The combiner processor of claim 77 where said accumulator includes a memory and an adder which adds the current said multiplier output to said memory contents.

100) The combiner processor of claim 77 where said decision output compares said accumulated value against a threshold at the end of said window.

101) The combiner processor of claim 100 where said threshold is 0.

102) The combiner processor of claim 1 where said codewords are used for direct sequence spread spectrum communications.

103) The combiner processor of claim 26 where said codewords are used for direct sequence spread spectrum communications.

104) The combiner processor of claim 52 where said codewords are used for direct sequence spread spectrum communications.

105) The combiner processor of claim 77 where said codewords are used for direct sequence spread spectrum communications.